## REMARKS

The application contains claims 1, 3-7 and 9-20. In view of the foregoing amendments and following remarks, Applicants respectfully request allowance of the application.

The objections to the title, drawings and claims 18-19 have been addressed with the foregoing amendments.

## THE CLAIMS DEFINE OVER THE CITED ART

Claim 1 has been amended to include the subject matter of originally presented claim 2, which had been rejected as obvious over Hennessy and Hoyt. Applicants respectfully submit that claim 2 is not obvious over the cited references because, even if their disclosures could be considered in combination, they would not suggest the claimed subject matter.

Claim 2 recites several elements, including:

> if the new instruction is a return instruction, ... determining whether a return address is available within the instruction pipe.
>
> stalling processing of the new instruction until valid data associated with the new instruction can be written to the next instruction pipestage,

The Office Action theorizes that, because Hoyt discloses a system that predicts return addresses, it would have been obvious to modify Hennessy's system to include this subject matter. Applicants respectfully disagree. Computer systems predict data values (say, a return address) to avoid having to wait for the actual value to be computed. If one were to use a predicted return address in Hennessy's system, there would be no stalling whatsoever. There would be no determination of whether the return address is available. The predicted return address would be available immediately and would permit the processing chain to be continue in an uninterrupted fashion. Claim 1, therefore, defines over this art. Claims 3-6 depend from claim 1 and also are allowable.

Claim 4 has been rewritten in independent form. It stands rejected as anticipated by Hennessy. Applicants respectfully request withdrawal of this rejection because Hennessy does not teach or suggest all elements of the pending claims. For, example, claim 4 recites:

> determining, with reference to other instructions read previously from the instruction pipestage, whether valid data associated with the new instruction can be written to a next instruction pipestage
>
> stalling processing of the new instruction until valid data associated with the new instruction can be written to the next instruction pipestage,
>
> wherein, if the new instruction is a call instruction, the determining includes determining whether immediate processing of the call instruction would exceed a predetermined access rate associated with a shared resource.

Hennessy does not disclose this subject matter. Respectfully, the Examiner has read the Hennessy's disclosure out of context. On page 142, Hennessy describes conflicts that occur during memory references (e.g., loads, fetches). Call instructions, however, do not reference a shared memory. The citation provided by the Office Actions (p. 277) as discussing call instructions clearly explains that the call instructions reference a dedicated buffer, which Hennessy calls a 'branch-target buffer' throughout pp. 271-278. Thus, Hennessy has not described any stalling operation that occurs when processing a call instruction. Claim 4 defines over this art.

Claim 7 has been amended to include the subject matter of original claim 8, which was rejected as obvious over Hennessy and Hoyt. Claim 7 recites:

> if the new instruction is a call instruction, after the stalling terminates, storing a return address associated with the call instruction both locally and in a shared resource.

Neither Hennessy nor Hoyt disclose storage of a return address in a shared resource. The Office Action alleges that stack 51 is a shared resource. Hoyt, however, never characterizes the stack 51 as being shared by any components. Thus, claim 7 defines over the art.

Applicants respectfully request withdrawal of the anticipation rejection to claim 10 because Hennessy does not teach or suggest all elements of that claim. Claim 10 recites:

> determining, with reference to other instructions read previously from the instruction pipestage, whether valid data associated with the new instruction is available to the instruction pipe prior to expiration of the round-trip communication latency period,

Claim 10 also explains that the latency period is a characteristic of an interface between an instruction pipe and an external resource. Hennessy does not teach or suggest this subject matter. The example cited in the Office Action is an example of data dependencies, not any round-trip communication latency. In Hennessy's case, the data is unavailable because it has

not been generated. In the circumstance of claim 10, even if the data is available in the external resource, it is unavailable to the instruction pipe because it cannot be communicated to the instruction pipe fast enough to be used. Accordingly, claim 10 is allowable over Hennessy.

Applicants respectfully request withdrawal of the anticipation rejection to claim 13. Claim 13 is an apparatus claim that defines a state machine and a clock control circuit each coupled to an output of the same instruction pipestage. The clock control circuit has an output for a modified clock signal which is input to the first pipestage and a second pipestage.

Hennessy does not disclose any clock control circuit whatsoever. Although he discloses stalling techniques in general, he does not disclose any apparatus that is used to implement such stalling. The Office Action's analysis infers that anticipatory subject matter may be present. Respectfully, this is inappropriate. If a reference does not expressly disclose the claimed subject matter, a rejection is proper only if the missing subject matter is present inherently. Inherency requires that there is no other way to perform the claimed subject matter. Here, this is not the case. Clock control may be achieved without requiring, for example, the state machine that controls it to be coupled to the first pipestage. Accordingly, the anticipation rejection to claim 13 must be withdrawn. Claims 14-16 also define over Hennessy.

Applicants respectfully request withdrawal of the rejection to claim 17. Claim 17 is directed to execution logic in a processor that includes multiple instruction pipestages, each of which is in communication with a common return stack buffer. The cited art does not each or suggest this subject matter. Skadron, in FIG. 4 does not disclose multiple instruction pipestages. Instead, FIG. 4 discloses two different sequences of ***program instructions*** that could be executed if a branch were incorrectly predicted. The program sequence takes the predicted path at the "while" instruction but ultimately the prediction is determined to be incorrect. All instructions in the predicted path are squashed when it is determined that the wrong path was taken. Program execution returns to the "while" instruction and resumes using the correct path.

Claim 17 clearly refers to multiple instruction pipes. These are circuit elements. Skadron does not teach multiple instruction pipes. It only describes multiple sequences of instructions. Therefore, claim 17 and claims 18-20 define over the art.

**CONCLUSION**

All claims are allowable over the cited art. Applicants, therefore, respectfully request allowance of the application.

Respectfully submitted,

Date: 8/15/03

Robert L. Hails, Jr.
Registration No. 39,702
(Attorneys for Intel Corporation)

KENYON & KENYON
1500 K Street, N.W.
Washington, D.C. 20005
Ph.: (202) 220-4200
Fax.: (202) 220-4201